AMENDMENTS

IN THE CLAIMS:

Please amend claims 2, 6-12, 19, and 20 as follows:

1. (Previously Presented) A method of stripping a hard mask from a substrate comprising an insulating material exposed within gaps patterned through the hard mask, comprising:

coating the substrate with a sacrificial material that fills the gaps; and

plasma etching to strip the sacrificial material and the hard mask substantially completely in a single plasma etch process.

2. (Currently Amended) The method of claim [[1]]19, wherein the hard mask material comprises a nitride.

3. (Original) The method of claim 2, wherein the hard mask material comprises SiN or SiON.

4. (Original) The method of claim 1, wherein the insulating material comprises an oxide.

5. (Original) The method of claim 1, wherein the insulating material comprises a material selected from the group consisting of silicon oxide, TEOS and HDP.

6. (Currently Amended) The method of claim [[1]]19, wherein the sacrificial material comprises a material selected from the group consisting of resists and organic BARC materials.

7. (Currently Amended) The method of claim [[1]]19, wherein the plasma etching is carried out with gases comprising a fluorinated hydrocarbon and oxygen.

8. (Currently Amended) The method of claim [[1]]19, wherein plasma etching completely removes the sacrificial material from the gaps.

9. (Currently Amended) The method of claim [[1]]19, wherein the sacrificial material is spin-coated onto the substrate.

10. (Currently Amended) ~~The method of claim 1,~~ A method of stripping a hard mask from a substrate comprising an insulating material exposed within gaps patterned through the hard mask, comprising:

coating the substrate with a sacrificial material that fills the gaps; and

plasma etching to strip the sacrificial material and the hard mask substantially completely in a single plasma etch process;

wherein the hard mask is employed to etch a layer or bulk portion of the substrate comprising silicon.

11. (Currently Amended) The method of claim [[1]]19, wherein the hard mask is employed to etch a silicon wafer.

12. (Currently Amended) The method of claim [[1]]19, wherein the hard mask is employed to etch a polysilicon or amorphous silicon layer.

13. (Original) The method of claim 10, wherein the hard mask material comprises a nitride.

14. (Original) The method of claim 13, wherein the hard mask material comprises SiN or SiON.

15. (Original) The method of claim 10, wherein the insulating material comprises an oxide.

16. (Original) The method of claim 10, wherein the sacrificial material comprises a material selected from the group consisting of resists and organic BARC materials.

17. (Original) The method of claim 10, wherein plasma etching completely removes the sacrificial material from the gaps.

18. (Original) The method of claim 10, wherein the sacrificial material is spin-coated onto the substrate.

19. (Currently Amended) A method of removing a hard mask from a silicon containing surface, comprising:

providing a sacrificial material that covers the hard mask[[s]] and fills gaps in the surface patterned with the hard mask; and

plasma etching to remove substantially completely the hard mask and that portion of the sacrificial material that covers the hard mask in a single plasma etch process.

20. (Currently Amended) The method of claim 19, wherein the sacrificial material protects an oxide within the gaps [[prior]] through at least a portion of the plasma etching.

21. (Previously Presented) A method of removing a hard mask, comprising:

forming an oxide region over a semiconductor substrate;

forming a silicon layer over the semiconductor substrate, wherein the silicon layer covers the oxide region;

forming and patterning a hard mask layer over the silicon layer;

etching a gap in the silicon layer to expose a portion of the oxide region using the patterned hard mask as an etch mask;

forming a sacrificial layer over the semiconductor substrate, thereby covering the hard mask layer and filling the gap;

removing substantially completely the sacrificial layer and the hard mask layer with a single dry etch, wherein an etch rate of the sacrificial layer and the hard mask layer is about the same, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

22. (Original) The method of claim 21, wherein the sacrificial layer comprises a BARC layer or a photoresist layer.

23. (Original) The method of claim 21, wherein forming the sacrificial layer comprises:

spinning coating the sacrificial layer over the semiconductor substrate; and

baking the sacrificial layer, thereby substantially planarizing the sacrificial layer.

24. (Previously Presented) A method of removing a hard mask comprising:

forming an oxide region over or within a semiconductor substrate;

forming a silicon layer over the semiconductor substrate, wherein the silicon layer covers the oxide region;

forming and patterning a hard mask layer over the silicon layer;

etching a gap in the silicon layer to expose a portion of the oxide region using the patterned hard mask as an etch mask;

forming a sacrificial layer having a relatively planar top surface over the semiconductor substrate, the sacrificial layer comprising a portion covering the hard mask layer and a portion filling the gap; and

removing substantially completely the sacrificial layer and the hard mask layer with a single plasma etch process, wherein an etch rate of the sacrificial layer and an etch rate of the hard mask layer are selected to substantially completely remove the portion of the sacrificial layer covering the hard mask and the hard mask layer, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

25-26. (Cancelled).

27. (Previously Presented) A method of stripping a hard mask from a substrate comprising an insulating material exposed within gaps patterned through the hard mask, comprising:

coating the substrate with a sacrificial material that fills the gaps; and

plasma etching to strip the sacrificial material and the hard mask in a single plasma etch process.